NOIS1SM1000A

STAR1000 1M Pixel Radiation Hard CMOS Image Sensor

ON Semiconductor®

http://onsemi.com

Features

- 1024 x 1024 Active Pixels
- 15 μm x 15 μm Pixel Size
- 1 inch – 35 mm Optical Format
- High Radiation Tolerance
- High Sensitivity
- Low Noise
- Monochrome and Color
- 11 Frames per Second (fps) at Full Resolution
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- Region of Interest (ROI) Readout
- Windowed and Subsampled Readout
- Rolling Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- Ceramic JLCC-84 Package
- BK7G18 Glass with N2 Filled Cavity
- 400 mW Power Dissipation
- These Devices are Pb−Free and are RoHS Compliant

Applications

Standard market Applications

- Nuclear Inspection

Space Applications

- Space Science
- Star Trackers
- Sun Sensors

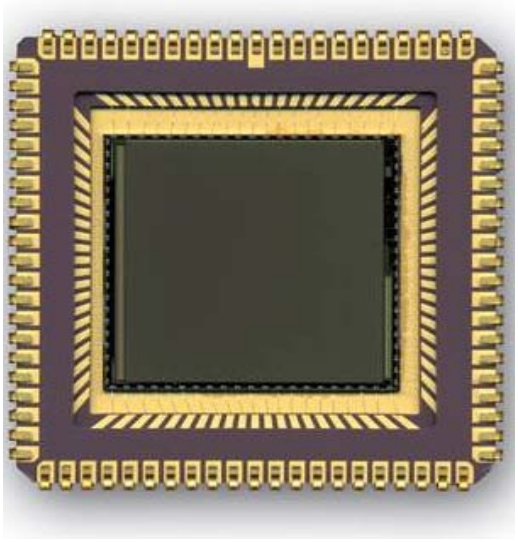

Figure 1. STAR1000 in 84−Pin Ceramic JLCC Package

JLDCC84
CASE 114AK

Description

The STAR1000 is a CMOS image sensor with 1024 by 1024 pixels on a 15 μm x 15 μm pitch. It features on-chip Fixed Pattern Noise (FPN) correction, a programmable gain amplifier, and a 10-bit Analog-to-Digital Converter (ADC).

All circuits are designed using the radiation tolerant design techniques to allow high tolerance against Radiation effects.

Registers which contain the X- and Y- addresses of the read out pixels can be directly accessed by the external controller. This architecture provides for flexible operation and allows different operation modes such as (multiple) windowing, subsampling, and so on.

The STAR1000 is assembled using a BK7G18 glass lid with a Nitrogen-filled cavity which increases the temperature operating range. The STAR1000 flight model has additional screening to space qualified standards.

ORDERING INFORMATION

Marketing Part Number	Description	Status	Package
NOIS1SM1000A-HHC	Mono with BK7G18 Glass, Engineering Model	Production	84 pin JLCC case 114AK
NOIS1SM1000S-HHC	Mono with BK7G18 Glass, Flight Model		
NOIS1SM1000A-HWC	Mono windowless, Engineering Model		
NOIS1SM1000S-HWC	Mono windowless, Flight Model	Risk Production	
NOIS1SC1000A-HHC	Color with BK7G18 Glass, Engineering Model	Engineering	

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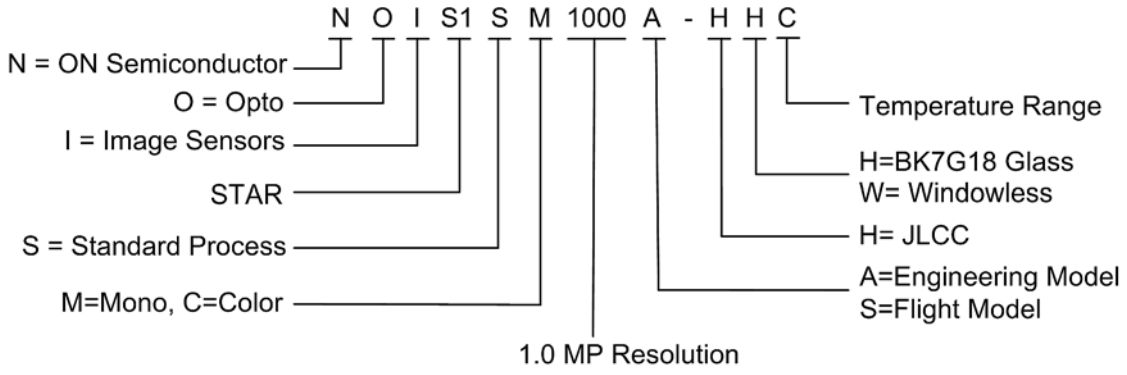
ORDERING CODE DECODER



Marking

The marking shall consist of a lead identification and traceability information.

Lead Identification

An index to pin 1 shall be located on the top of the package as shown in section Package Dimensions on page 21. The pin numbering is counter clock-wise, when looking at the top-side of the component.

Traceability Information Tests

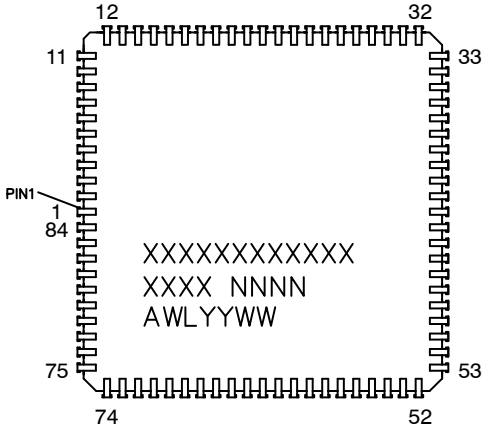
Each component shall be marked such that complete traceability can be maintained.

The component shall bear a number that is constituted as follows:

Orderable Part Number	Package Mark: Line 1	Package Mark: Line 2	Package Mark: Line 3
NOIS1SM1000A-HHC	NOIS1SM1000A	-HHC NNNN	AWLYYWW
NOIS1SM1000S-HHC	NOIS1SM1000S	-HHC NNNN	AWLYYWW
NOIS1SM1000A-HWC	NOIS1SM1000A	-HWC NNNN	AWLYYWW
NOIS1SC1000A-HHC*	NOIS1SC1000A	-HHC NNNN	AWLYYWW
where NNNN- serialized number controlled manually by ON Semiconductor, BELGIUM			
where AWLYYWW represents the lot assembly date			

*The NOIS1SC1000A−HHC is in engineering sample.

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
NNNN = Serial Number

INTRODUCTION

Overview

This specification details the ratings, physical, geometrical electrical and electro-optical characteristics, test and inspection data for a CMOS Active Pixel image Sensor (CMOS APS) based on type STAR 1000. The sensor has a format of 1024 by 1024 pixels on a 15 μm x 15 μm pitch, and contains an on-chip 10-bit ADC.

This specification shall be read in conjunction with the ESCC generic specification ESCC 9020 issue 2 dated March 2010.

Export Clearance

The STAR1000 is subject to export clearance for some countries and applications, and an export license might be required.

Component Type Variants

A summary of the type variants of the basic CMOS image sensor is shown in the ordering information. The complete list of detailed specifications for each type option is listed in the acceptance criteria specification.

All specifications presented in this datasheet are rated at 22 ±3°C, under nominal clocking and bias conditions. Exceptions are noted in the 'remarks' field.

Soldering instructions

Soldering is restricted to manual soldering only. No wave or reflow soldering is allowed. For the manual soldering, following restrictions are applicable:

- Solder 1 pin on each of the 4 sides of the sensor
- Cool down period of min. 1 minute before soldering another pin on each of the 4 sides
- Repeat soldering of 1 pin on each side, including a 1 minute cool down period.

Handling precautions

The component is susceptible to damage by electro-static discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling. The following guidelines are applicable:

- Always manipulate the devices in an ESD controlled environment
- Always store the devices in a shielded environment that protects against ESD damage (at least a non-ESD generating tray and a metal bag)
- Always wear a wrist strap when handling the devices and use ESD safe gloves.

The STAR1000 is classified as class 1A (JEDEC classification – [AD03]) device for ESD sensitivity.

For proper handling and storage conditions, refer to ON Semiconductor application note AN52561, Image Sensor Handling and Best Practices.

Storage information

The components must be stored in a dust-free and temperature-, humidity and ESD controlled environment.

- Devices must always be stored in special ESD-safe trays such that the glass window is never touched.
- The trays are closed with EDS-safe rubber bands
- The trays are sealed in an ESD-safe conductive foil in clean room conditions.
- For transport and storage outside a clean room the trays are packed in a second ESD-save bag that is sealed in clean room.

Limited Warranty

ON Image Sensor Business Unit warrants that the image sensor products to be delivered hereunder, if properly used and serviced, will conform to Seller's published specifications and will be free from defects in material and workmanship for two (2) years following the date of shipment. If a defect were to manifest itself within two (2) years period from the sale date, ON Semiconductor will either replace the product or give credit for the product.

Return Material Authorization (RMA)

ON Semiconductor packages all of its image sensor products in a clean room environment under strict handling procedures and ships all image sensor products in ESD-safe, clean-room-approved shipping containers. Products returned to ON Semiconductor for failure analysis should be handled under these same conditions and packed in its original packing materials, or the customer may be liable for the product.

APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

No.	Reference	Title	Issue	Date
AD01	ESCC Generic Specification 9020	Charge Coupled Devices, Silicon, Photosensitive	2.0	March 2010
AD02	CISP spec# 001-06225	Electro-optical test methods for CMOS image sensors	E	October, 2008
AD03	JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	B	June, 2000
AD04	APS-FF-SC-03-010	Process Identification Document	3.0	
AD05	CISP spec# 001-49283	Visual Inspection for FM devices	1	January, 2008

NOTE: CISP # – CMOS Image Sensor Products, ON Semiconductor

TERMS, DEFINITIONS ABBREVIATIONS, SYMBOLS AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC basic Specification 21300 shall apply.

The following formulas are applicable to convert %Vsat and mV/s into e- and e-/s:

- $FPN[e^-] = \frac{FPN[\%Vsat] * \overline{Vsat}}{conversion\_gain}$
- $Dark\_signal[e^-/s] = \frac{Dark\_signal[V/s]}{conversion\_gain}$
- $DSNU[e^-] = \frac{DSNU[\%Vsat] * \overline{Vsat}}{conversion\_gain}$
- Conversion gain for STAR1000: 11.5 μV/e-

TEST PROCEDURE OVERVIEW

Environmental and Endurance Tests

Electrical and electro−opticalmeasurements on completion of environmental test

The parameters to be measured on completion of environmental tests are scheduled in Table 21. Unless otherwise stated, the measurements shall be performed at an environmental temperature of 22 ±3°C. Measurements of dark current are performed at 22 ±1°C and the actual environmental temperature must be reported with the test results.

Electrical and electro−optical measurements at intermediate point during endurance test

The parameters to be measured at intermediate points during endurance test of environmental tests are scheduled in Table 21. Unless otherwise stated, the measurements shall be performed at an environmental temperature of 22 ±3°C.

Electrical and electro−opticalmeasurements on completion of endurance test

The parameters to be measured on completion of endurance tests are scheduled in Table 21. Unless otherwise stated, the measurements shall be performed at an environmental temperature of 22 ±3°C.

Conditions for operating life test

The conditions for operating life tests shall be as specified in Table 20 of this specification.

Electrical circuits for operating life test

Circuits for performing the operating life test are shown in Figure 2 of this specification.

Conditions for high temperature storage test

The temperature to be applied shall be the maximum storage temperature specified in Table 6 of this specification.

Lot Acceptance and Screening

Lot acceptance and screening are based on the ESA basic specification ESCC 9020.

This paragraph describes the LAT and screening for the STAR1000 flight model devices.

Table 1. WAFER LOT ACCEPTANCE (on every fab lot)

Test	Test Method	Number of Devices	Test Condition	Test Location
Wafer processing data review	PID	NA	NA	ON Semiconductor
SEM	ESCC 21400	4 devices	NA	Test House
Total dose test	ESCC 22900	3 devices	See below	Test House by ON Semiconductor
Endurance test	MIL-STD-883 Method 1005	6 devices	See below	Test House

Total dose test conditions performed on unscreened devices:

- NOIS1SM1000S-HHC 100KRad at 3.6 Krad/hour max dose rate, and biased

Endurance test conditions performed on unscreened devices:

- NOIS1SM1000S-HHC 2000h, biased at +125°C

Following tests will be performed before and after total dose testing and endurance tests.

Table 2. ASSEMBLY LOT ACCEPTANCE

Test	Test Method	Number of Devices	Test Condition	Test Location
Special assembly house in process control				Assembly House
Bond strength test	MIL-STD-883 method 2011	2	D	Assembly House
Assembly house geometrical data	Review	All		ON SEMI
Solderability Terminal strength Marking permanence	MIL-STD883, method 2003 MIL-STD 883, method 2004 ESCC 24800	3	D	Test House
Geometrical measurements	ICD	All		ON SEMI
Temperature cycling	MIL-STD 883, method 1010	5	B 50 Cycles −55°C/+125°C	Test House
Moisture resistance	JEDEC STD Method 1018.3	2	Procedure 1	Test House
DPA				
Die shear test	MIL-STD-883 method 2019	4	N/A	Test House
Bond pull test	MIL-STD-883 method 2011		All wires	Test House

Before and after the following tests are done:

- Electrical testing at high, low and room temperature. This testing is performed in accordance with the ICD.
- Detailed visual inspection in accordance with CISP# spec 001-49283
- Fine Leak test MIL-STD-883, Test Method 1014, Condition A
  - Pass condition is < 5 x 10-7 atms. cm3/s
- Gross Leak test MIL-STD-883, Test Method 1014, Condition C
  - Pass condition is no bubbles visible during test

NOTE: As the glass lid needs to be removed in order to perform the DPA, this test cannot be guaranteed to be 100% successful.

Table 3. PERIODIC TESTING

As stated in the ESCC 9020, periodic testing is performed every 2 years. The following tests are part of the periodic testing.

Test	Test Method	Number of Devices	Test Condition	Test Location
Mechanical shock	MIL-STD 883, Method 2002	2	B - 5 shocks, 1500g – 0.5 ms – 1/2 sine, 6 axes, 30 shocks total	Test House
Mechanical vibration	MIL-STD 883, Method 2007	2	A - 4 Cycles, 20g 80 to 2000 Hz, 0.06 inch 20 to 80 Hz, 3 axes, 12 Cycles total	Test House
DPA				
Die shear test	MIL-STD-883 method 2019	2	N/A	Test House
Bond pull test	MIL-STD-883 method 2011		All wires	Test House

Before and after the mechanical testing the following testing is performed.

- Electrical verification test at room temperature.
- Detailed visual inspection in accordance with CISP# spec 001-49283
- Geometrical measurements
- Fine Leak test MIL-STD-883, Test Method 1014, Condition A
  - Pass condition is < 5x 10-7 atms. cm3/s
- Gross Leak test MIL-STD-883, Test Method 1014, Condition C
  - Pass condition is no bubbles visible during test

NOTE: As the glass lid needs to be removed in order to perform the DPA, this test cannot be guaranteed to be 100% successful.

Table 4. SCREENING

Test	Test Method	Number of Devices	Test Condition	Test Location
Electrical testing at high, low and room temperature	CISP spec# 001-66578	All	HT +85°C LT –40°C RT +25°C	ON Semiconductor
Geometrical measurements		All		ON Semiconductor
Visual inspection	CISP spec# 001-49283	All		ON Semiconductor
Stabilization bake	MIL-STD-883 method 1008	All	48h at 125°C	Test House
XRAY	ESCC 20900	All		Test House
Fine leak test	MIL-STD-883 method 1014	All	A	Test House
Gross leak test	MIL-STD-883 method 1014	All	C	Test House
Temperature cycling	MIL-STD-883 method 1010	All	B - 10 cycles –55°C / +125°C	Test House
Biased Burn-in		All	240h at +125°C.	ON Semiconductor
Mobile Particle Detection	MIL-STD-883 method 2020	All	A	Test House
Fine leak test	MIL-STD-883 method 1014	All	A	Test House
Gross leak test	MIL-STD-883 method 1014	All	C	Test House
Electrical testing at high, low and room temperature	CISP spec# 001-66578	All	HT +85°C LT –40°C RT +25°C	ON Semiconductor
Final Visual Inspection	CISP spec# 001-49283	All		ON Semiconductor

SPECIFICATIONS

Table 5. ACCEPTANCE CRITERIA KEY SPECIFICATION

Defective pixels	20
Bright pixels in FPN image	20
Defective pixels in PRNU image	50
Defective columns	0
Defective rows	0
Allowed adjacent bright pixels	2
Allowed cluster size of 4 or more bright pixels	0
DSNU defects @ 22°C BOL	108

NOTE: A detailed acceptance criteria specification is available upon request.

Table 6. MINIMUM / MAXIMUM RATINGS

Characteristics	Limits		Units
	Min	Max	
Any supply voltage	-0.5	+5.5	V
Voltage on any input terminal	-0.5	Vdd +0.5	V
Operating temperature	-40	+85	°C
Storage temperature	-55	+125	°C
Soldering temperature	NA	260	°C

NOTE: Engineering model option is guaranteed for room temperature only.

NOTE: Stresses above these ratings may cause permanent damage. A 7V peak for very short durations is sustainable, but exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note AN52561.

Table 7. GENERAL SPECIFICATIONS

Characteristics	Limits
Image sensor format	1024 by 1024 pixels
Pixel size	15 μm by 15 μm
ADC resolution	10 bit

Table 8. MECHANICAL SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Units
Die (Referring to Figure 3: Die Optical Center)	Die thickness (applicable to STAR 1000 mono)	488	508	528	μm
	Die thickness (applicable to STAR 1000 color)	605	625	645	μm
	Flatness of the image area			10	μm
	Die center, X offset to the center of package	0.002	0.052	0.102	mm
	Die center, Y offset to the center of the package	0.1	0.2	0.3	mm
	Die position, X tilt	(-0.1)	0	(0.1)	deg
	Die position, Y tilt	(-0.1)	0	(0.1)	deg
	Die placement accuracy in package	(-50)	-	(+50)	μm
	Die rotation accuracy	-1	-	1	deg
	Optical center referenced from package center (X-dir)	(-50)	0	(+50)	μm
	Optical center referenced from package center (Y-dir)	(-50)	0	(+50)	μm
Package	Package weight	7.7	7.85	8	g
	Package thickness (Package + epoxy + glass lid), not including lead height	3.3	3.45	3.6	mm

Table 9. GLASS LID SPECIFICATIONS

No.	Characteristic	Min	Typ	Max	Unit	Remarks
1a	XY size	26.7 x 26.7	26.8 x 26.8	26.9 x 26.9	mm	
1b	Thickness	1.4	1.5	1.6	mm	
2a	Spectral range for optical coating of window	440	NA	1100	nm	
2b	Reflection coefficient for window	NA	<0.8	<1.3	%	Over bandwidth indicated in 2a
3	Optical quality: Scratch max width Scratch max number Dig max size Dig max number	N/A	N/A	 10 5 60 25	μm	

Total Dose Radiation Test

Application

The total dose radiation test shall be performed in accordance with the requirements of ESCC Basic specification 22900.

Parameter drift values

The allowable parameter drift values after total dose irradiation are listed in Table 17. The parameters shown are valid after a total dose of 270 KRad and 168h/100°C annealing.

Bias conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 2 of this specification.

Electrical and electro-optical measurements

The parameters to be measured, prior to, during and on completion of the irradiation are listed in Table 21 of this specification. Only devices that meet the specification in Table 21 of this specification shall be included in the test sample.

Table 10. RADIATION INFLUENCE

Characteristics	Limits			Units
	Min	Typ	Max	
Operating temperature range	-40	NA	+85	°C
Total dose radiation tolerance (device in operation)	270	NA	NA	Krad (Si)
Equivalent proton influence	$2.4E^{11}$	NA	NA	Proton/cm^2
SEL threshold	127.8	NA	NA	MeV cm^3 mg^{-1}

Electrical and electro-optical measurements

Electrical and Electro-Optical measurements at high and low temperature

The engineering model option is screened for room temp only, while the flight model option is screened over the full guaranteed temperature range.

Circuits for electrical and electro-optical measurements

A Circuit for performing the electro-optical tests shown below is shown in Figure 2.

Table 11. ELECTRICAL CHARACTERISTICS

(under nominal bias conditions at nominal pixel rate with Tj = 22 ±3°C in “soft reset”, unless otherwise stated)

Characteristics	Limits			Units
	Min	Typ	Max	
Total power supply current stand-by		53.8	56.6	mA
Total power supply current, operational		57.4	60.8	mA
Power supply current to ADC, operational		44.6	48	mA
Power supply current to image core, operational		12.8	14	mA
Input impedance digital input	200			KΩ
Input impedance Dark Reference input	200			KΩ
Input impedance ADC input	200			KΩ
Output impedance digital outputs. (Note 1)		200 – 700		Ω
Output impedance analog output. (Note 1)			100	Ω
Output amplifier voltage range	0.5		4.5	V
Dark reference offset. (Note 2)		0.6	0.93	V
Output amplifier gain setting 1. (Note 3)	3.95	4.45	4.96	
Output amplifier gain setting 2. (Note 3)	2.05	2.30	2.55	
Output amplifier gain setting 3. (Note 3)	7.36	8.38	9.40	
ADC ladder network resistance	1054	1174	1295	Ω
ADC ladder network temperature coefficient for temperature range −40°C to +85°C		4.53		Ω/°C
ADC Differential non linearity		3.89	8.4	LSB
ADC Integral non linearity		1.29	1.95	LSB
ADC set-up time to attain 1% conversion accuracy			250	ns
ADC delay time			72	ns

1. The output impedance varies for different digital outputs and is dependent on the metal routing, where D9 has the longest routing and D0 has the shortest routing, providing a typical range of 200-700 ohms inclusive of the ESD resistance.
2. Dark reference offset specifies the offset between the applied dark reference voltage and the actual level at the analogue output terminal. Specified at gain setting 0.
3. Gain specification relative to gain setting 0.

Table 12. ELECTRO−OPTICAL INFORMATION
(under nominal bias conditions at nominal pixel rate with Tj = 22 ±3°C in “soft reset”, unless otherwise stated)

Characteristics	Limits			Units
	Min	Typ	Max	
Saturation voltage output	0.99	1.11	1.24	V
Linear range (within ±1%)		95		Ke-
Full well charge (Note 1)		135		Ke-
Quantum efficiency x Fill factor (Between 450 nm and 750 nm)		30		%
Responsivity narrow band blue, at 475 nm ±20 nm	21000	25300		ADU
Responsivity narrow band green, at 526 nm ±20 nm	20500	24800		ADU
Responsivity narrow band red, at 630 nm ±20 nm	18400	23000		ADU
Charge to voltage conversion factor. (Note 2)		11.5		mV/e-
Temporal noise, at 5 MHz clock rate		0.61	0.72	mV
Temporal noise, at 2 MHz clock rate		0.77	1.02	mV
Temporal noise, at 10 MHz clock rate		0.82	1.13	mV
Local fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 3)		0.13	0.20	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 4)		0.38	0.62	$\%V_{sat}$
Local fixed pattern noise standard deviation, at 2 MHz clock rate. (Note 3)		0.20	0.27	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 2 MHz clock rate. (Note 4)		0.42	0.55	$\%V_{sat}$
Local fixed pattern noise standard deviation, at 10 MHz clock rate. (Note 3)		0.21	0.33	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 10 MHz clock rate. (Note 4)		0.39	0.78	$\%V_{sat}$
Column FPN. (Note 5)		0.37	0.61	$\%V_{sat}$
Average dark signal		13.5	28.2	mV/s
Dark signal temperature dependency (temperature rise for doubling average dark current)		9.2		°C
Local dark signal non uniformity standard deviation		0.79	1.03	$\%V_{sat}$
Global dark signal non uniformity standard deviation		0.99	1.32	$\%V_{sat}$
Local photo response non uniformity, standard deviation. (Note 6)		0.95	1.33	%
Global photo response non uniformity, standard deviation. (Note 7)		3.30	6.09	%
MTF X direction. (Note 8)		0.26		
MTF Y direction. (Note 8)		0.37		
Pixel to pixel cross talk X direction. (Note 9)		17.5		%
Pixel to pixel cross talk Y direction. (Note 9)		16		%
Anti-blooming capability		X 1000		

1. Full well charge and linear range are calculated from detailed electro-optical response measurements.
2. Charge to voltage conversion factor is calculated from the detailed electro-optical response measurements.
3. Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.
4. Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.
5. Percentage of full well charge, measured in the complete FPA area
6. Percentage of signal (black offset subtracted), measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window PRNUs.
7. Percentage of signal (black offset subtracted), measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.
8. MTF is calculated from the detailed electro-optical response measurements.
9. Pixel to pixel optical crosstalk in percentage of charge in illuminated pixel.

Table 13. ELECTRICAL AND ELECTRO−OPTICAL MEASUREMENTS AT REFERENCE TEMPERATURE

The limits in this table set the acceptance criteria for procurement of samples.

Characteristics	Limit Min	Limit Max	Units
Contact test, ESD input structures	No fail	No fail	
Total power supply current stand-by		56.0	mA
Total PS current, operational		60.1	mA
PS current ADC, operational		47.3	mA
PS current to image core, operational		13.8	A
Offset 0	-100	100	mV
Output amplifier gain setting 1. (Note 1)	4.02	5.01	
Output amplifier gain setting 2. (Note 1)	2.07	2.58	
Output amplifier gain setting 3. (Note 1)	7.57	9.42	
ADC ladder network resistance	1078	1271	Ω
ADC Differential non linearity	NA	8.36	LSB
ADC Integral non linearity	NA	1.82	LSB
Saturation voltage output	1.01	NA	V
Responsivity narrow band blue	21900	NA	ADU
Responsivity narrow band green	21400	NA	ADU
Responsivity, narrow band red	19300	NA	ADU
Temporal noise, nom. clock frequency		0.75	mV
Temporal noise, red. clock frequency		0.97	mV
Temporal noise, enhanced clock freq.		1.07	mV
Local fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 2)		0.22	%Vsat
Global fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 3)		0.57	%Vsat
Local fixed pattern noise standard deviation, at 2 MHz clock rate. (Note 2)		0.25	%Vsat
Global fixed pattern noise standard deviation, at 2 MHz clock rate. (Note 3)		0.52	$\%V_{sat}$
Local fixed pattern noise standard deviation, at 10 MHz clock rate. (Note 2)		0.34	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 10 MHz clock rate. (Note 3)		0.70	$\%V_{sat}$
Column FPN. (Note 4)		0.56	$\%V_{sat}$
Average dark signal		25.3	mV/s
Local DSNU standard deviation		0.98	$\%V_{sat}$
Global DSNU standard deviation		1.26	$\%V_{sat}$
Local PRNU, standard deviation. (Note 5)		1.25	%
Global PRNU, standard deviation. (Note 6)		5.53	%

1. Gain specification relative to gain setting 0.
2. Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.
3. Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.
4. Percentage of full well charge, measured in the complete FPA area.
5. Percentage of signal (black offset subtracted), measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window PRNUs.
6. Percentage of signal (black offset subtracted), measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

Table 14. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT +85°C

Characteristics	Limit min	Limit max	Units
Total power supply current stand-by		56.6	mA
Total PS current, operational		60.6	mA
PS current ADC, operational		47.7	mA
PS current to image core, operational		13.9	A
ADC ladder network resistance	1341	1576	Ω
Saturation voltage output	1.05		V
Responsivity narrow band blue	22100		ADU
Responsivity narrow band green	21500		ADU
Responsivity, narrow band red	19600		ADU
Temporal noise, at 10 MHz clock rate		2.37	mV
Average dark signal		950	mV/s
Local DSNU standard deviation		1.02	$\%V_{sat}$
Global DSNU standard deviation		2.84	$\%V_{sat}$
Number of DSNU signal defects		NA	
Local PRNU, standard deviation. (Note 3)		1.30	%
Global PRNU, standard deviation. (Note 4)		4.31	%

Table 15. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS AT −40°C

Characteristics	Limit min	Limit max	Units
Total power supply current stand-by		60.0	mA
Total PS current, operational		63.9	mA
PS current ADC, operational		51.1	mA
PS current to image core, operational		13.2	A
ADC ladder network resistance	770	1013	Ω
Saturation voltage output	1.01		V
Responsivity narrow band blue	22100		ADU
Responsivity narrow band green	22200		ADU
Responsivity, narrow band red	19700		ADU
Temporal noise, at 10 MHz clock rate.		0.60	mV
Local fixed pattern noise standard deviation, at 10 MHz clock rate. (Note 1)		0.22	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 10 MHz clock rate. (Note 2)		0.41	$\%V_{sat}$
Average dark signal			mV/s
Local DSNU standard deviation			$\%V_{sat}$
Global DSNU standard deviation			$\%V_{sat}$
Number of DSNU signal defects			
Local PRNU, standard deviation. (Note 3)		1.25	%
Global PRNU, standard deviation. (Note 4)		5.94	%

1. Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.
2. Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.
3. Percentage of signal (black offset subtracted), measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window PRNUs.
4. Percentage of signal (black offset subtracted), measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

Table 16. ELECTRICAL CHARACTERISTICS

The min and max limits of Table 3 apply

Table 17. PARAMETER DRIFT VALUES FOR RADIATION TESTING AT 22 ±1 °C

Characteristics	Limits			Units
	Min	Typ	Max	
Average dark signal rise		252	424	e^-/s per Krad
Local dark signal non uniformity rise		5	10	e^-/s per Krad
Global dark signal non uniformity rise		6	14	e^-/s per Krad

Table 18. PROTON RADIATION DRIFT VALUES

Characteristics	Limits			Units
	Min	Typ	Max	
Average dark signal, at 22 ±1°C		35		mV/s
Local dark signal non uniformity standard deviation		2.5		%
Global dark signal non uniformity standard deviation		2.7		%

Table 19. CONDITIONS FOR HIGH TEMPERATURE REVERSE BIAS BURN−IN

Not applicable

Table 20. CONDITIONS FOR POWER BURN-IN AND OPERATING LIFE TESTS

Characteristics	Symbol	Test condition	Units
Ambient temperature	Tamb	125C	°C
All power supplies	Vdd	+5.5	V
Bias conditions		See Figure 2	
X clock frequency		5	MHz

Table 21. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS ON COMPLETION OF ENVIRONMENTAL TESTS AND AT INTERMEDIATE POINTS AND ON COMPLETION OF ENDURANCE TESTING

Characteristics	Limit Min	Limit Max	Units
Contact test, ESD input structures	No fail	No fail	
Total power supply current stand-by		56.0	mA
Total PS current, operational		60.1	mA
PS current ADC, operational		47.3	mA
PS current to image core, operational		13.8	A
Offset 0	-100	100	mV
Output amplifier gain setting 1. (Note 1)	4.02	5.01	
Output amplifier gain setting 2. (Note 1)	2.07	2.58	
Output amplifier gain setting 3. (Note 1)	7.57	9.42	
ADC ladder network resistance	1078	1271	Ω
ADC Differential non linearity		8.36	LSB
ADC Integral non linearity		1.82	LSB
Saturation voltage output	1.01		V
Responsivity narrow band blue	21900		ADU
Responsivity narrow band green	21400		ADU
Responsivity, narrow band red	19300		ADU
Temporal noise, at 5 MHz clock rate		0.75	mV
Temporal noise, at 2 MHz clock rate		0.97	mV
Temporal noise, at 10 MHz clock rate		1.07	mV
Local fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 2)		0.22	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 3)		0.57	$\%V_{sat}$
Local fixed pattern noise standard deviation, at 2 MHz clock rate. (Note 2)		0.25	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 2 MHz clock rate. (Note 3)		0.52	$\%V_{sat}$
Local fixed pattern noise standard deviation, at 10 MHz clock rate. (Note 2)		0.34	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 10 MHz clock rate. (Note 3)		0.70	$\%V_{sat}$
Column FPN. (Note 4)		0.56	$\%V_{sat}$
Average dark signal		25.3	mV/s
Local DSNU standard deviation		0.98	$\%V_{sat}$
Global DSNU standard deviation		1.26	$\%V_{sat}$
Local PRNU, standard deviation. (Note 5)		1.25	%
Global PRNU, standard deviation. (Note 6)		5.53	%

1. Gain specification relative to gain setting 0.
2. Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.
3. Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.
4. Percentage of full well charge, measured in the complete FPA area.
5. Percentage of signal (black offset subtracted), measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window PRNUs.
6. Percentage of signal (black offset subtracted), measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

Table 22. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS DURING AND ON COMPLETION OF TOTAL-DOSE IRRADIATION TESTING

Characteristics	Limit Max	Units
Total power supply current stand-by	56.0	mA
Total PS current, operational	60.1	mA
Local fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 1)	0.22	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 2)	0.57	$\%V_{sat}$
Number of FPN signal defects	Table 17	
Average dark signal	Table 17	
Local DSNU standard deviation	Table 17	
Global DSNU standard deviation	Table 17	

Table 23. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS DURING AND ON COMPLETION OF PROTON IRRADIATION TESTING

Proton irradiation testing is performed with 2.4E11 protons at energy of 60 Mev.

Characteristics	Limit Max	Units
Total power supply current stand-by	56.0	mA
Total PS current, operational	60.1	mA
Local fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 1)	0.22	$\%V_{sat}$
Global fixed pattern noise standard deviation, at 5 MHz clock rate. (Note 2)	0.57	$\%V_{sat}$
Number of FPN signal defects	Table 5	
Average dark signal	Table 17	
Local DSNU standard deviation	Table 17	
Global DSNU standard deviation	Table 17	

1. Percentage of full well charge, measured in complete FPA area. Local specification indicates variation of pixel values with respect to the average of a 20 x 20 window area. The number given is the average of all 20 x 20 window FPNs.
2. Percentage of full well charge, measured in complete FPA area. Global specification indicates variation of pixel value with respect to global average.

Table 24. ELECTRICAL AND ELECTRO-OPTICAL MEASUREMENTS DURING AND ON COMPLETION OF HEAVY ION IRRADIATION TESTING

Characteristics	Limit Min	Limit Max	Units
Total power supply current stand-by		56.0	mA
Total PS current, operational		60.1	mA

During heavy ion testing no specific tests or measurement are executed. Instead the image sensors are operated at nominal speed and power supply current is monitored.

Heavy ion testing is performed with a total dose of 10E7 particles with an effective LET of 127.8 MeV/mg/cm2.

Burn−in Test

Parameter drift values

The parameter drift values for power burn-in are specified in Table 13 of this specification. Unless otherwise specified the measurements shall be conducted at an environmental temperature of 22 ±3°C and under nominal power supply, bias and timing conditions.

The parameter drift values (Δ) shall not be exceeded. In addition to these drift value requirements, also the limit values of any parameter as indicated in Table 13 shall not be exceeded.

Conditions for high temperature reverse bias burn-in

Not Applicable

Conditions for power burn-in

The conditions for power burn-in shall be as specified in Table 20 of this specification

Electrical circuits for high temperature reverse bias burn-in

Not applicable

Electrical circuits for power burn-in

Circuits to perform the power burn-in test are shown in Figure 2 of this specification.

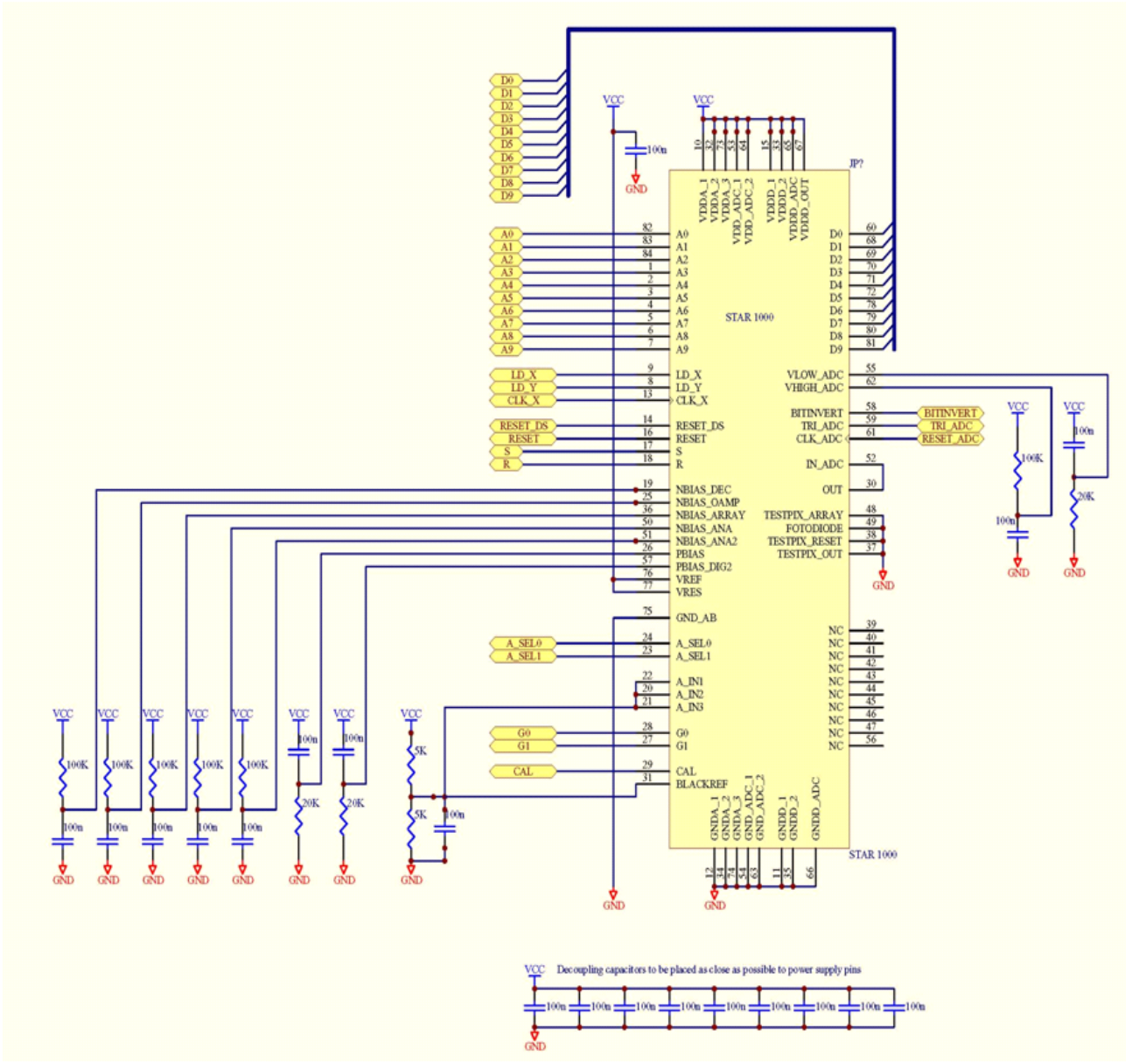


Figure 2. STAR1000 Functional Diagram
(used for biasing, burn in, life and electro optical measurements)

MECHANICAL SPECIFICATIONS

Dimension check

The dimensions of the components specified herein shall be checked. They shall comply with the specifications and the tolerances as indicated in Figure 3 and in section Package Dimensions on page 21.

Geometrical characteristics

The geometrical characteristics of the components specified herein shall be checked. They shall comply with the specifications and the tolerances as indicated in section Package Dimensions on page 21.

Weight

The maximum weight of the components specified herein shall be as specified in Table 8.

Materials and finishes

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used.

Case

The case shall be hermetically sealed and have a ceramic body and a glass window.

Type	JLCC-84
Material	Black Alumina BA-914
Thermal expansion coefficient	7.6 x 10^{-6} /K
Hermeticity	< 5 x 10E-7 atm cc/s
Thermal resistance (Junction to case)	3.633 °C/W

Lead material and finish

Lead Material	KOVAR
1e Finish	Nickel, min 2 μm
2nd Finish	Gold, min 1.5 μm

Window

The window material shall be BK7G18 with anti-reflective coating applied on both sides. The window has a coating free border of 1.5 mm on both sides at each border.

Refer to Table 8 for the anti−reflective coating specification and Table 9 for the glass defect criteria.

A detailed drawing of the window is given in Figure 3.

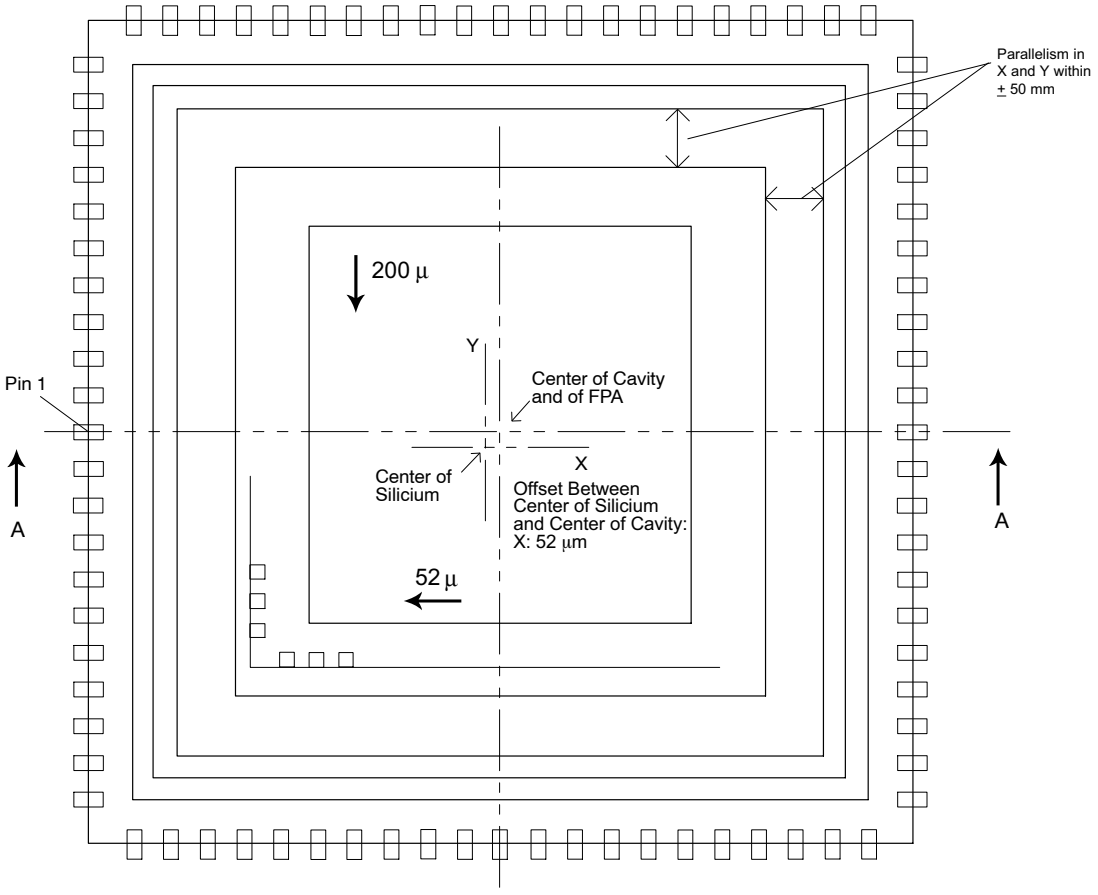


Figure 3. Die Optical Center

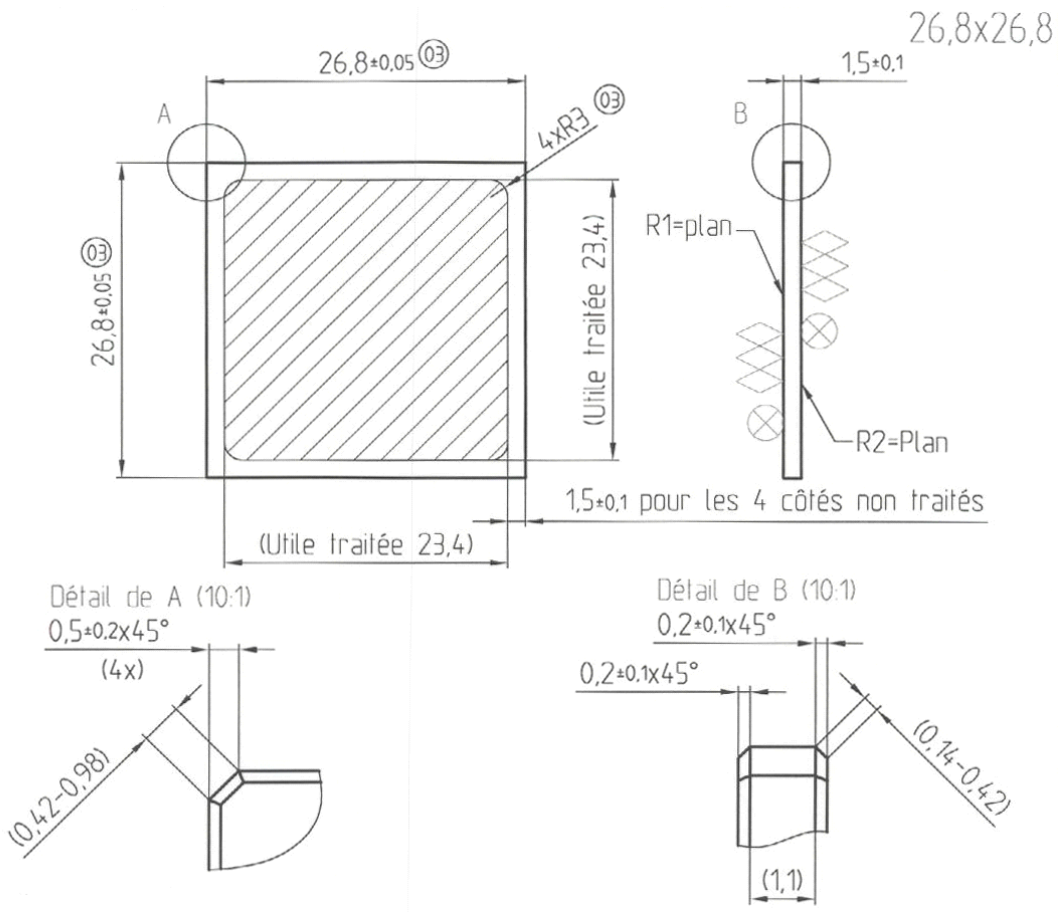
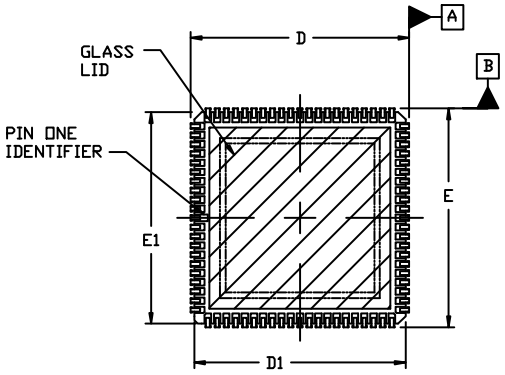


Figure 4. Glass Lid Dimensions

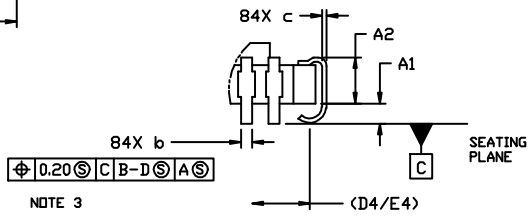
PACKAGE DIMENSIONS

JLDCC84
CASE 114AK
ISSUE A



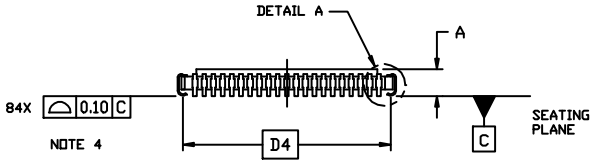
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUMS A, B, AND D ARE DETERMINED AT DATUM C. POSITION OF THE LEADS IS DETERMINED AT DATUM C.
4. COPLANARITY APPLIES TO THE LOWEST PART OF THE LEAD.

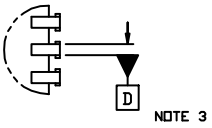


DETAIL A

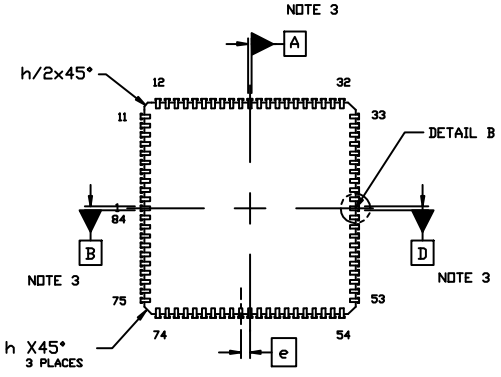
DIM	MILLIMETERS	
	MIN.	MAX.
A	3.77	4.57
A1	0.51	---
A2	2.16 REF	
b	0.46	0.56
c	---	0.20
D	30.08	30.38
D1	28.96	29.46
D4	28.70 BSC	
E	30.08	30.38
E1	28.96	29.46
E4	28.70 BSC	
e	1.27 BSC	
h	0.90	1.15



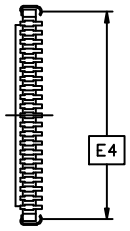
SIDE VIEW



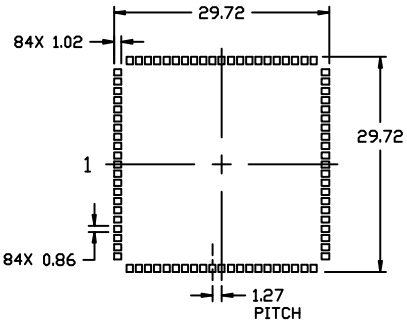
DETAIL B



BOTTOM VIEW



END VIEW



RECOMMENDED MOUNTING FOOTPRINT

PIN DESCRIPTION

This appendix contains a pin description for the STAR1000 CMOS image sensor.

Table 25. PIN LIST

Pin	Pin Name	Pin Type	Pin Description
1	A3	Input	
2	A4	Input	
3	A5	Input	
4	A6	Input	
5	A7	Input	
6	A8	Input	
7	A9	Input	
8	LD_Y	Input	Digital Input. Latch address (A0…A9) to Y-register (0 = track, 1 = hold).
9	LD_X	Input	Digital input. Latch address (A0…A9) to X-register (0 = track, 1 = hold).
10	VDDA	Supply	Analog power supply of the imager (typical 5 V).
11	GNDD	Ground	Digital ground of the imager.
12	GNDA	Ground	Analog ground of the imager.
13	CLK_X	Input	Digital input. Clock X-register (output valid & stable when CLK_X is high).
14	RESET_DS	Input	Digital input (active high). Resets row indicated by Y-address (see sensor timing diagram). RESET_DS is used for dual-slope integration (see FAQ). GND is used for normal operation.
15	VDDD	Supply	Digital supply of the image sensor.
16	RESET	Input	Digital input (active high). Resets row indicated by Y-address (see sensor timing diagram).
17	S	Input	Digital input (active high). Control signal for column amplifier (see sensor timing diagram).
18	R	Input	Digital input (active high). Control signal for column amplifier (see sensor timing diagram).
19	NBIAS_DEC	Input	Analog input. Biasing of address decoder. Connect with 100 kΩ to VDDA and decouple with 100 nF to GND.
20	A_IN2	Input	Additional analog inputs. For proper conversion with on-chip ADC, the input signal must lie within the output signal range of the image sensor (approximately +2 V to +4 V).
21	A_IN3	Input	
22	A_IN1	Input	
23	A_SEL1	Input	Selection of analog channel: ‘00’ selects image sensor (‘01’ selects A_IN1, ‘10’ A_IN2, and ‘11’ A_IN3).
24	A_SEL0	Input	
25	NBIAS_OAMP	Input	Analog input. Bias of output amplifier (speed/power control). Connect with 100 kΩ to VDDA and decouple with 100 nF to GND for 12.5 MHz output rate (lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation).
26	PBIAS	Input	Analog input. Biasing of the multiplexer circuitry. Connect with 20 kΩ to GND and decouple with 100 nF to VDD.
27	G1	Input	Digital input. Select output amplifier gain value: G0 = LSB, G1 = MSB (‘00’ = unity gain, ‘01’ = x2, ‘10’ = x4, ‘11’ = x8).
28	G0	Input	
29	CAL	Input	Digital input (active high). Initialization of output amplifier. Output amplifier outputs BLACKREF in unity gain mode when CAL is high (1). Apply pulse pattern (see sensor timing diagram).
30	OUT	Output	Analog Output Video Signal. Connected to the analog input of the internal (pin 52) 10-bit ADC or an external ADC.

Table 25. PIN LIST

Pin	Pin Name	Pin Type	Pin Description
31	BLACKREF	Input	Analog input. Control voltage for output signal offset level. Buffered on-chip, the reference level can be generated by a 100 kΩ resistive divider. Connect to 2 V DC for use with on-chip ADC.
32	VDDA	Supply	Analog power supply of image core (typical 5 V).
33	VDDD	Supply	Digital power supply of image core (typical 5 V).
34	GNDA	Ground	Analog ground of image core.
35	GNDD	Ground	Digital ground of image core.
36	NBIAS_ARRAY	Input	Analog input. Biasing of the pixel array. Connect with 1MΩ to VDDA and decouple with 100 nF capacitor to GND.
37	NC		Pins 37 through 47 are No Connects.
38	NC		
39	NC		
40	NC		
41	NC		
42	NC		
43	NC		
44	NC		
45	NC		
46	NC		
47	NC		
48	TESTPIXARRAY	Output	Analog output of an array of 20 x 35 test pixels where all photodiodes are connected in parallel. Is used for electro-optical evaluation.
49	PHOTODIODE	Output	Plain Photo Diode (without circuitry). Area of the photodiode = 20 x 35 pixels. Is used for electro-optical evaluation.
50	NBIAS_ANA	Input	Analog input. Analog biasing of the ADC circuitry. Connect with 100 kΩ to VDDA and decouple with 100 nF to GND.
51	NBIAS_ANA2	Input	
52	IN_ADC	Input	Analog input of the internal ADC. Connect to analog output of image sensor (pin 30). Input range (typically 2 V and 4 V) of the internal ADC is set between by VLOW_ADC (pin 55) and VHIGH_ADC (pin 62).
53	VDD_ADC_ANA	Supply	Analog power supply of the ADC (typical 5 V).
54	GND_ADC_ANA	Ground	Analog ground of the ADC.
55	VLOW_ADC	Input	Low reference voltage of internal ADC. Nominal input range of the ADC is between 2 V and 4 V. The resistance between VLOW_ADC and VHIGH_ADC is approximately 1.5 kΩ. Connect with 1.5 kΩ to GND and decouple with 100 nF to GND.
56	NC		
57	PBIASDIG2	Input	Connect with 20 kΩ to GND and decouple with 100 nF to VDDA.
58	BITINVERT	Input	Digital input. Inversion of the ADC output bits. 0 = invert output bits (0 => black, 1023; white, 0), 1 = no inversion of output bits (black, 0; white, 1023).
59	TRI_ADC	Input	Digital input. Tri-state control of digital ADC outputs (1 = tri-state, 0 = normal mode).
60	D0	Input	ADC output bits.#D0 = LSB, D9=MSB.
61	CLK	Input	Digital input. ADC clock. ADC converts on falling edge.
62	VHIGH_ADC	Input	High reference voltage of internal ADC. Nominal input range of the ADC is between 2 V and 4 V. The resistance between VLOW_ADC and VHIGH_ADC is about 1.5 kΩ. Connect with 1.1 kΩ to VDDA and decouple with 100 nF to GND.

Table 25. PIN LIST

Pin	Pin Name	Pin Type	Pin Description
63	GND_ADC_ANA	Ground	Analog ground of the ADC circuitry.
64	VDD_ADC_ANA	Supply	Analog supply of the ADC circuitry (typical 5 V).
65	VDD_ADC_DIG	Supply	Digital supply of the ADC circuitry (typical 5 V).
66	GND_ADC_DIG	Output	Digital ground of the ADC circuitry.
67	VDD_DIG_OUT	Supply	Power supply of ADC digital output. Connect to 5 V for normal operation. Can be brought to lower voltage when image sensor must be interfaced to low voltage periphery.
68	D1	Output	ADC output bits. #D0 = LSB, D9 = MSB.
69	D2	Output	
70	D3	Output	
71	D4	Output	
72	D5	Output	
73	VDDA	Supply	Analog supply of the image core (typical 5 V).
74	GNDA	Ground	Analog ground of the image core (typical 5 V).
75	GND_AB	Supply	Anti-blooming drain control voltage. Default: connect to ground where the anti-blooming is operational but not maximal. Apply 1 V DC for improved anti-blooming.
76	VREF	Supply	Analog supply. Reset level for RESET_DS. Is used for extended optical dynamic range. See FAQ for more details.
77	VRES	Supply	Analog supply. Reset level for RESET (typical 5 V).
78	D6	Output	ADC output bits. #D0 = LSB, D9 = MSB.
79	D7	Output	
80	D8	Output	
81	D9	Output	
82	A0	Input	Digital input. Address inputs for row and column addressing. A9 = LSB, A0 = MSB.
83	A1	Input	
84	A2	Input	

ARCHITECTURE

Floor Plan

The image sensor contains five sections: the pixel array, the X- and Y- addressing logic, the column amplifiers, the output amplifier and the ADC. Figure 4 shows an outline diagram of the sensor, including an indication of the main control signals. The following paragraphs explain the function and operation of the different imager parts in detail.

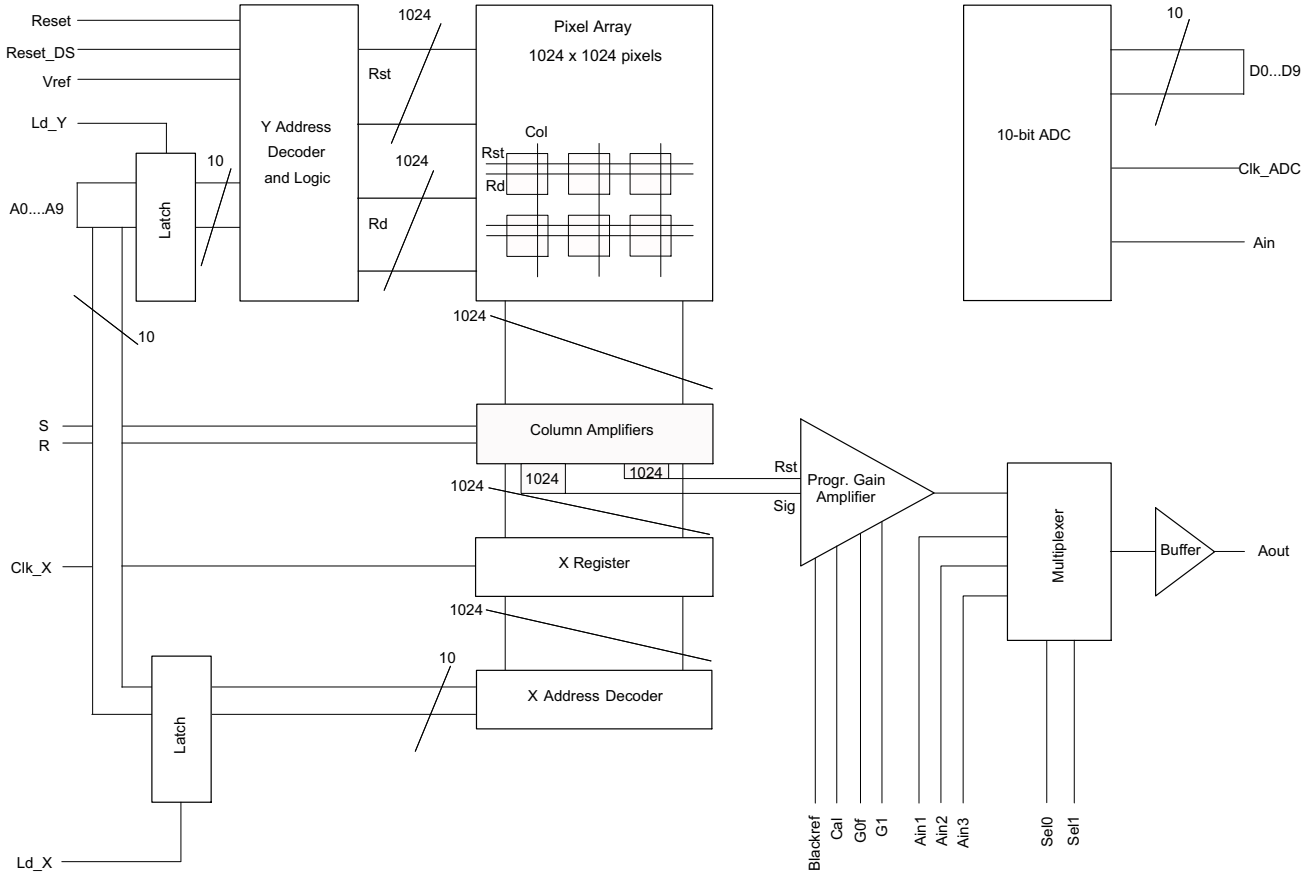


Figure 5. Image Sensor Architecture

Pixel Array

The pixel array contains 1024 by 1024 active pixels at 15 mm pitch. Each pixel contains one photo diode and three transistors as shown in Figure 5.

The photo diode is always in reverse bias. At the beginning of the integration cycle, a pulse is applied to the reset line (gate of T1) bringing the cathode of D1 to the reset voltage level. During the integration period, photon-generated electrons accumulate on the diode capacitance reducing the voltage on the gate of T2. The real illumination dependent signal is the difference between the reset level and the output level after integration. This difference is created in the column amplifiers. T2 acts as a source follower and T3 allows connection of the pixel signal (reset level and output level) to the vertical output bus.

The reset lines and the read lines of the pixels in a row are connected together to the Y- decoder logic; the outputs of the pixels in a column are connected together to a column amplifier.

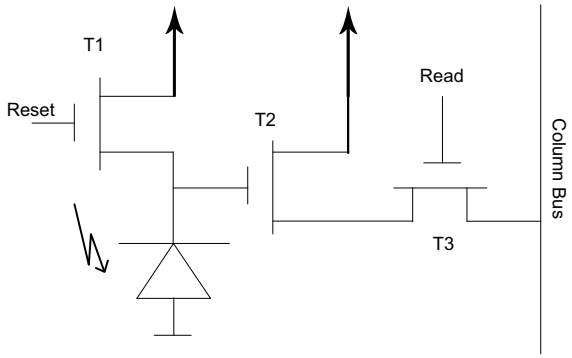


Figure 6. 3T Pixel Architecture

Addressing Logic

The addressing logic allows direct addressing of rows and columns. Instead of the one-hot shift registers that are often used, address decoders are implemented. One can select a line by presenting the required address to the address input of the device and latching it to the Y- decoder logic. Presenting the
X- address to the device address input and latching it to the X- address decoder can select a column.

A typical line read out sequence first selects a line by applying the Y-address to the Y-decoder. Activation of the LD_Y input on the Y-logic connects the pixel outputs of the selected line to the column amplifiers. The individual column amplifier outputs are connected to the output amplifier by applying the respective
X- addresses to the X- address decoder. Applying the appropriate Y- address to the Y- decoder and activating the "Reset" input reset a line. The integration time of a row is the time between the last reset of this row and the time when it is selected for read out.

The Y- decoder logic has two different reset inputs: RESET and RESET_DS. Activation of RESET resets the pixel to the Vdd level; activation of RESET_DS resets the pixel to the voltage level on the VREF input. This feature allows the application of the so called dual slope integration. If dual slope integration is not needed, VREF is tied to Vdd and RESET_DS must never be activated.

Column Amplifiers

All outputs from the pixels in a column are connected in parallel to a column amplifier. This amplifier samples the output voltage and the reset level of the pixel whose row is selected at that moment and presents these voltage levels to the output amplifier. As a result, the pixels are always reset immediately after read out as part of the sample procedure. Note that the maximum integration time of a pixel is the time between two read cycles.

Output Amplifier and Analog Multiplexer

The output amplifier combines subtraction of pixel signal level from reset level with a programmable gain amplifier. Because the amplifier is AC coupled, it also contains a provision to maintain and restore the proper DC level.

An analog signal multiplexing feeds the pixel signal to the final unity gain buffer, providing the required drive capability. Apart from the pixel signal, three other external analog signals can be fed to the output buffer. All these signals can be digitalised by the on-chip ADC if the output of this buffer is externally connected to the input of the ADC.

The purpose of the additional analog inputs (A_IN1, A_IN2, and A_IN3) is to allow the possibility of processing other analog signals through the image sensors signal path. These signals can then be converted by the ADC and processed by the image controller FPGA. The additional analog inputs are intended for low frequency or DC signals and have a reduced bandwidth compared with the image signal path.

ADC

The image sensor has a 10-bit ADC that is electrically separated from the rest of the image sensor circuits and can be powered down if an external ADC is used. The conversion takes place at the falling edge of the clock and the output pins can be disabled to allow operation of the device in a bus structure.

Bayer Pattern

The STAR1000 is available in a color variant. Looking from Top View, with Pin 1 left center, pixel red is (0,0) as shown in Figure 6.

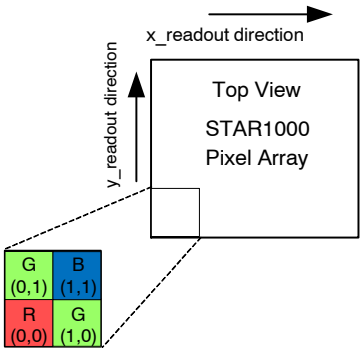


Figure 7. Bayer Pattern for STAR1000

TIMING AND CONTROL SIGNALS

The pixels addressing is done by direct addressing of rows and columns. This approach has the advantage of full flexibility when accessing the pixel array: multiple windowing and subsampled read out are possible by proper programming.

The following paragraphs clarify the timing for row and column readout.

Row Selection and Reset Timing

Figure 7 shows the timing of the line sequence control signals. The timing constraints are presented in Table 26.

The address, presented at the address IO pins is latched in with the LD-Y pulse.

After latching, the external controller already produces a new address.

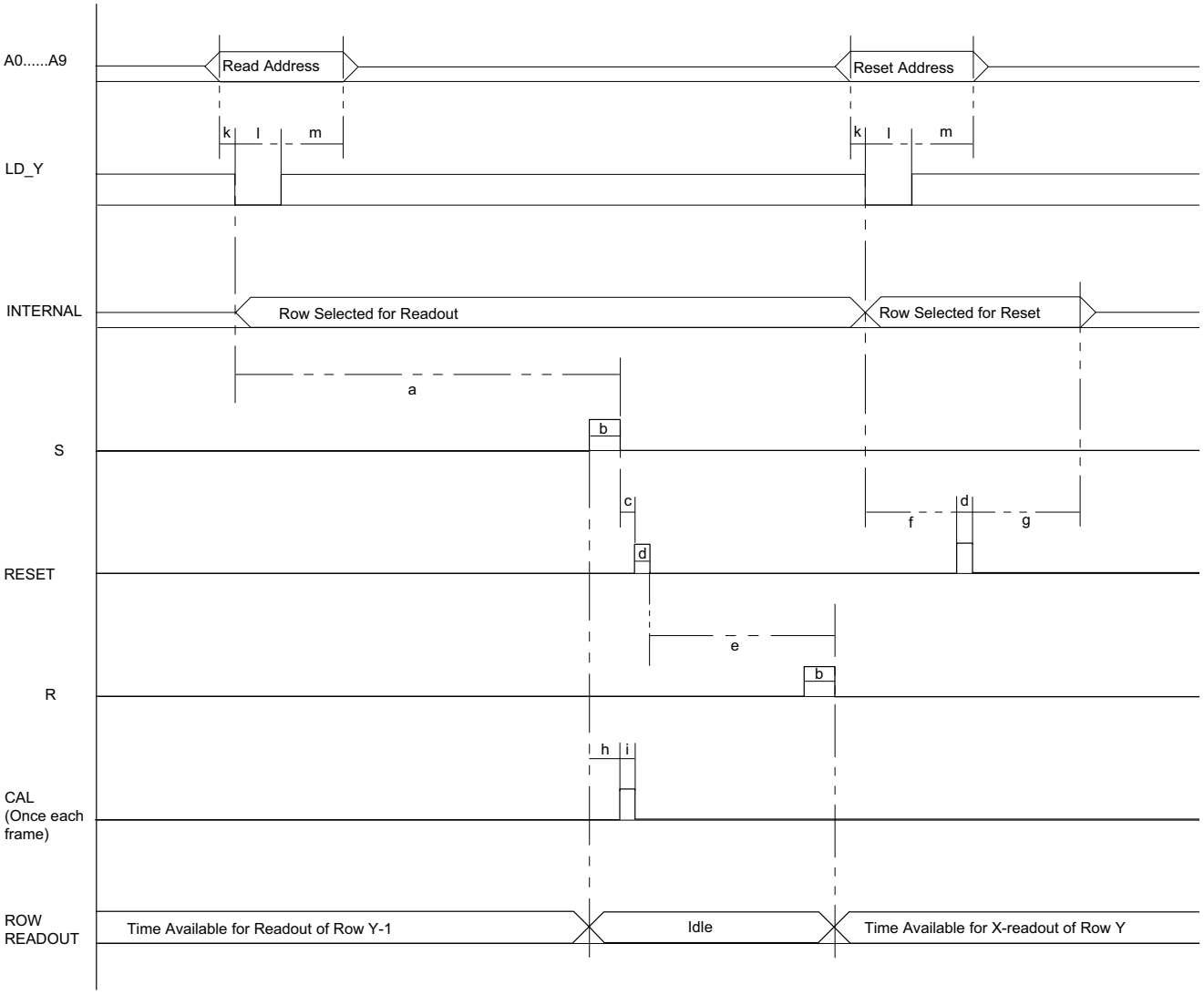


Figure 8. Line Selection and Reset Sequence

Latching in a Y- address selects the addressed row and connects the pixel outputs of that row to the column amplifiers. Through the sequence of the S and R pulse and the reset pulse in between the pixel output signal and reset level are sampled and produced at the output of the column amplifier.

At this time horizontal read out of the selected row is started and another row is reset to effectuate reduced integration time.

Below table shows the timing constraints for the horizontal or line-select timing. The given data are based upon the results of simulations.

Table 26. TIMING CONSTRAINTS OF LINE SEQUENCE

Symbol	Min	Typ	Description
a	3.6 μs		Delay between selection of a new row and falling edge on S. Minimal value: For maximum, speed a new row can already be selected during X- read out of the previous row.
b	0.4 μs		Duration of S and R pulse.
c	0	100 ns	Delay between falling edge of S and rising edge of reset.
d	200 ns		Minimum duration of reset pulse.
e	1.6 μs		Delay between falling edge of reset and falling edge of R.
f	0	100 ns	Minimum delay between falling edge on LD_Y and rising edge of reset.
g		g	Minimum required extension of Y- address after falling edge of reset pulse.
h	100 ns	200 ns	Position of cal pulse after rising edge of S. The cal pulse must only be given once per frame.
i	100 ns	1 μs	Duration of cal pulse.
k	10 ns		Address set up time.
l	20 ns		Load register value.
m	10 ns		Address stable after load.

Pixel Read Out Timing

Figure 8 shows the timing of the pixel readout sequence. The external digital controller presents a column address that is latched by the rising edge of the LD_X pulse. After decoding the X- address the column selection is clocked in the X- register by CLK-X. The output amplifier uses the same pulse to subtract the pixel output level from the pixel reset level and the signal level. This causes a pipeline effect such that the analog output of the first pixel is effectively present at the device output terminal at the third rising edge of the X-CLK signal.

The ADC conversion starts at the falling edge of the CLK-ADC signal and produces a valid digital output 20 ns after this edge. The timing constraints are given in Table 27.

Important note: The values of the X shift-register tend to leak away after a while. Therefore, it is very important to keep the CLK_X signal asserted for as long as the sensor is powered up. If the sensor sits idle and CLK_X is not asserted, the leakage of the X shift-register causes multiple columns to be selected at once. This forces high current through the sensor and may cause damage.

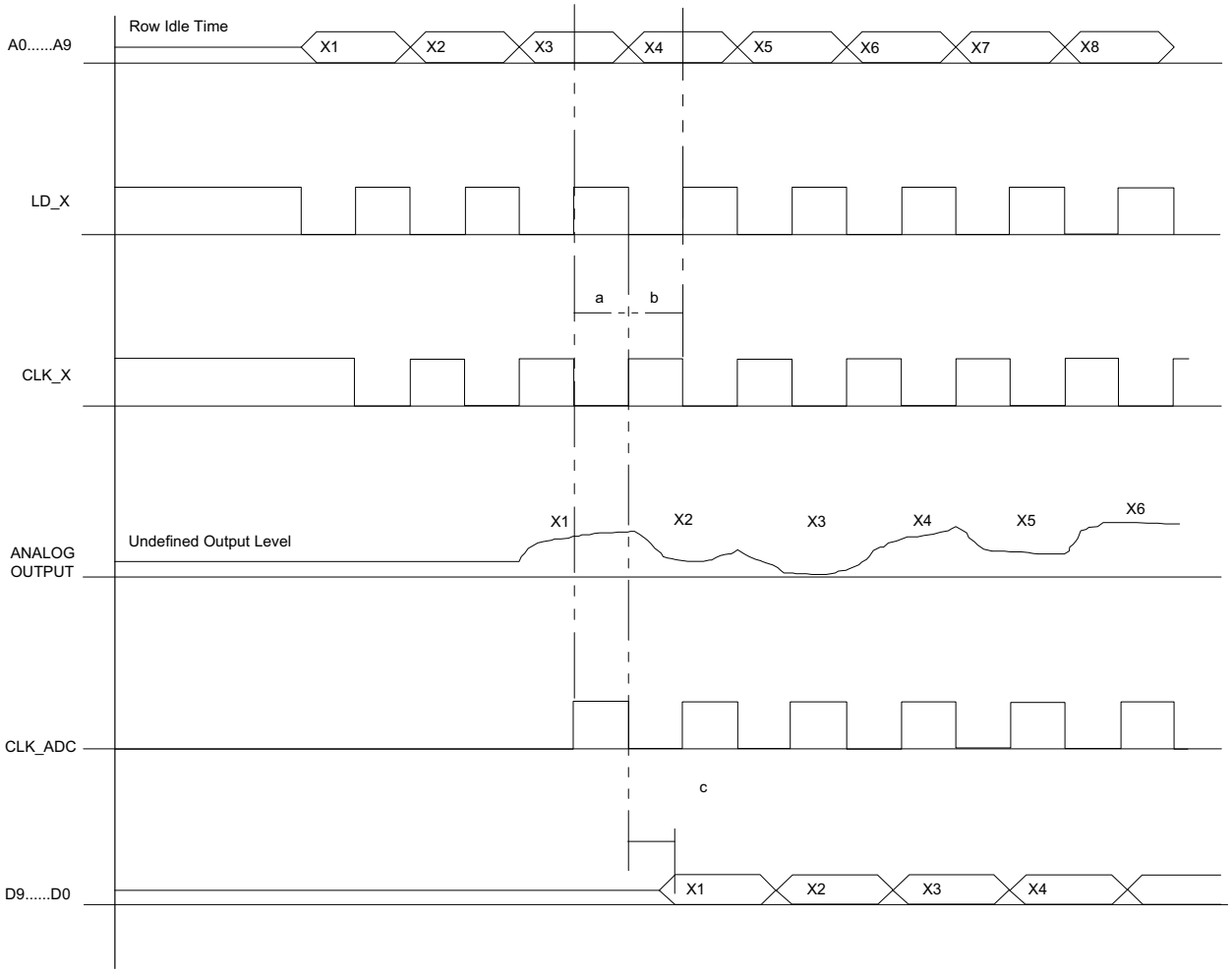


Figure 9. Column Selection and Read Out Sequence

Table 27. TIMING CONSTRAINTS OF COLUMN READ OUT

Symbol	Min	Typ	Description
a	20 ns		Address setup time
b	40 ns		Address valid time
c	0	20 ns	ADC output valid after falling edge of CLK_ADC

APPENDIX A: TYPICAL SPECTRAL RESPONSE DATA

The following figure shows a typical spectral response curve. The fringes in the curve result from optical interference in the top dielectric layers.

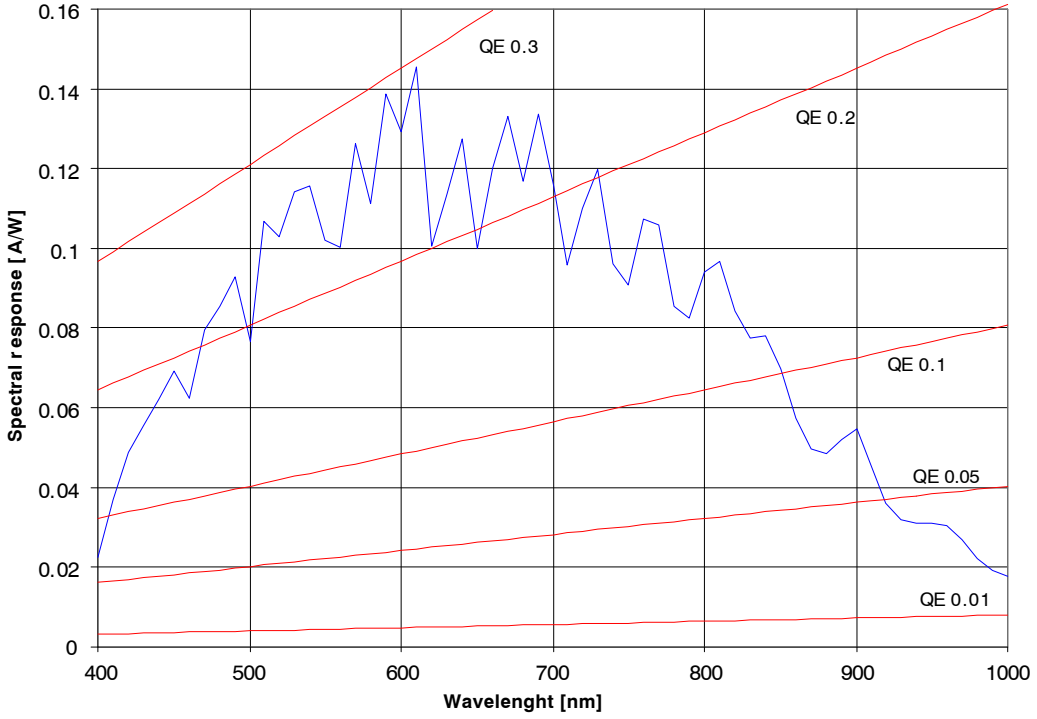


Figure 10. Spectral Response

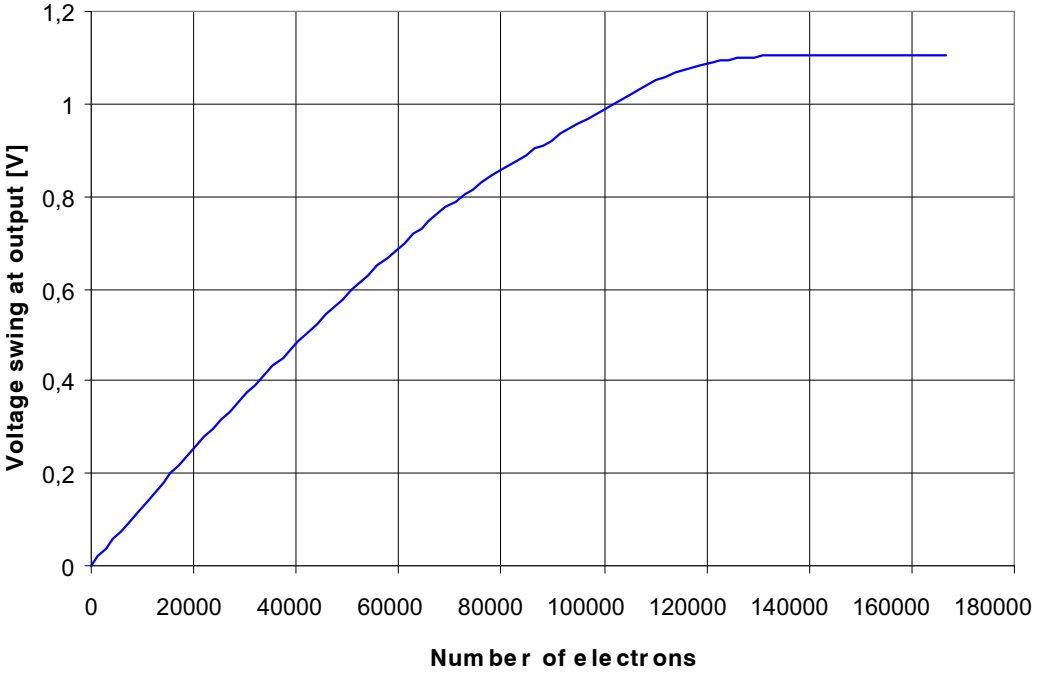


Figure 11. Photovoltaic Response

APPENDIX B: TYPICAL PIXEL PROFILE DATA

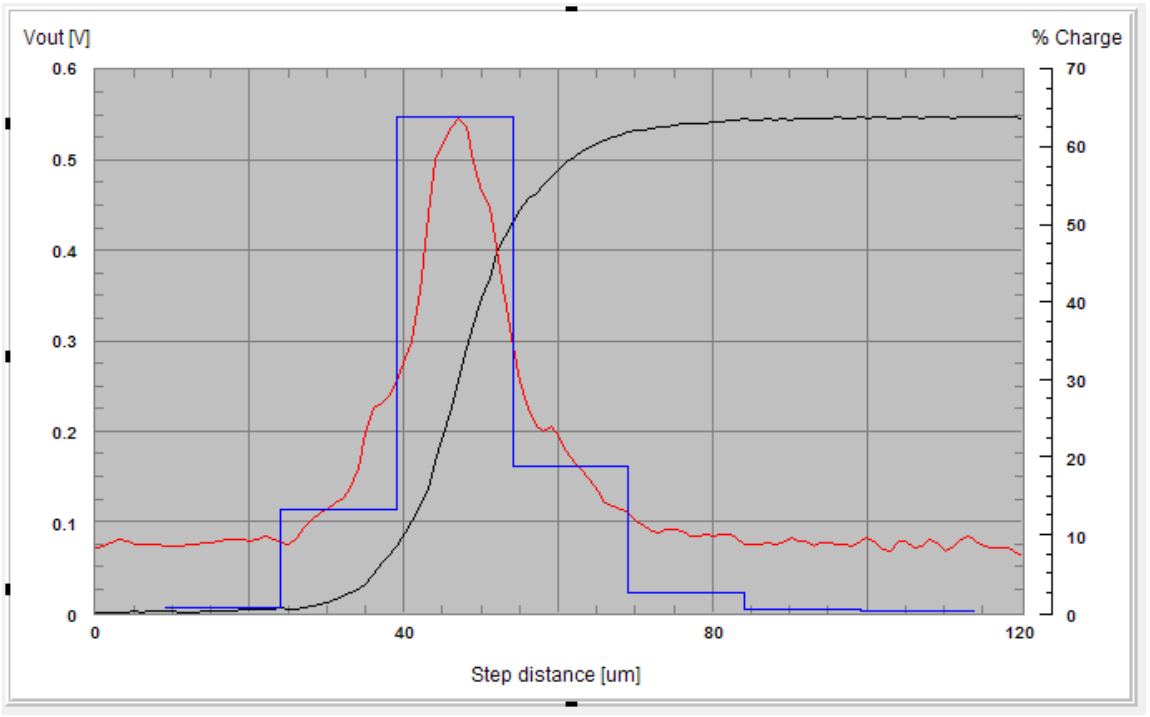


Figure 12. Vertical pixel profile measurement data at 600 nm.

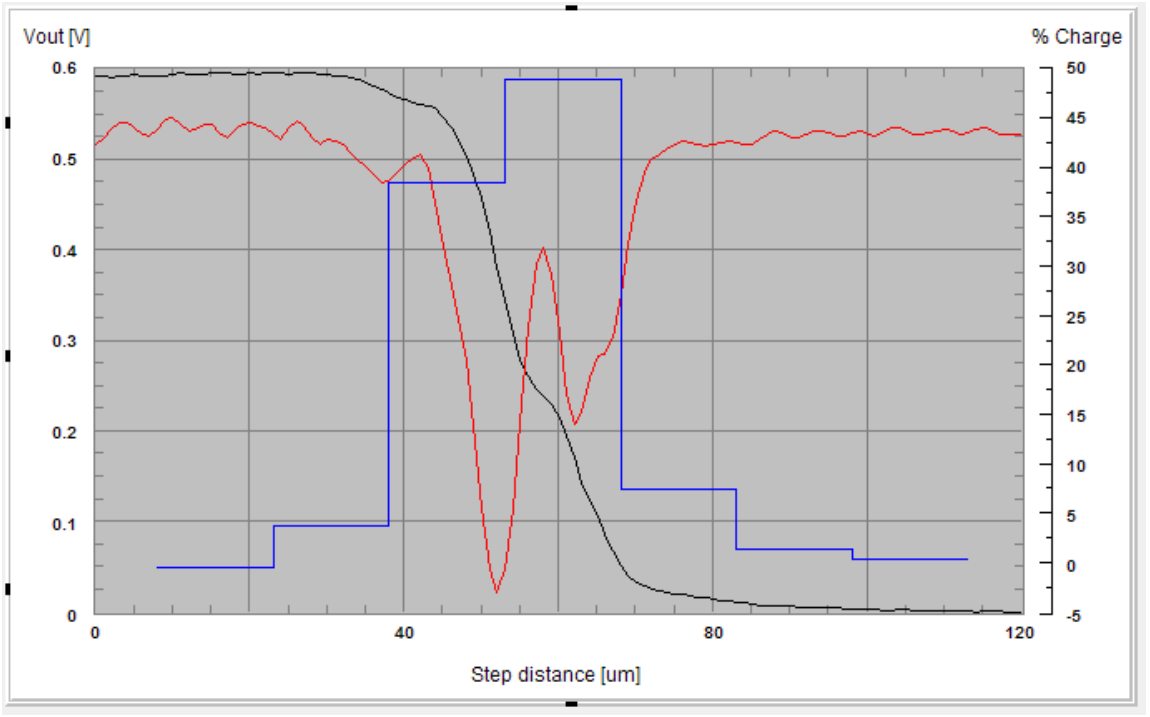


Figure 13. Horizontal pixel profile measurement data at 600 nm.

APPENDIX C: OBSERVED EFFECTS DURING ANNEALING AFTER TOTAL DOSE IRRADIATION

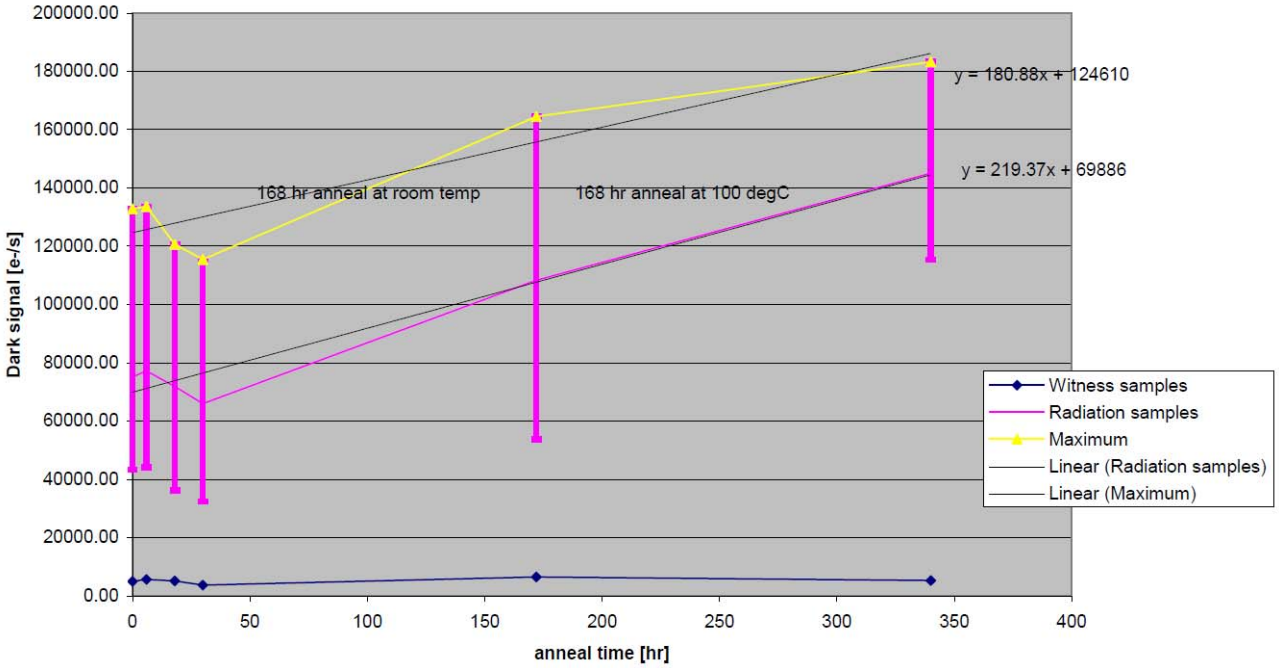


Figure 14. STAR1000 Average Dark Current during annealing

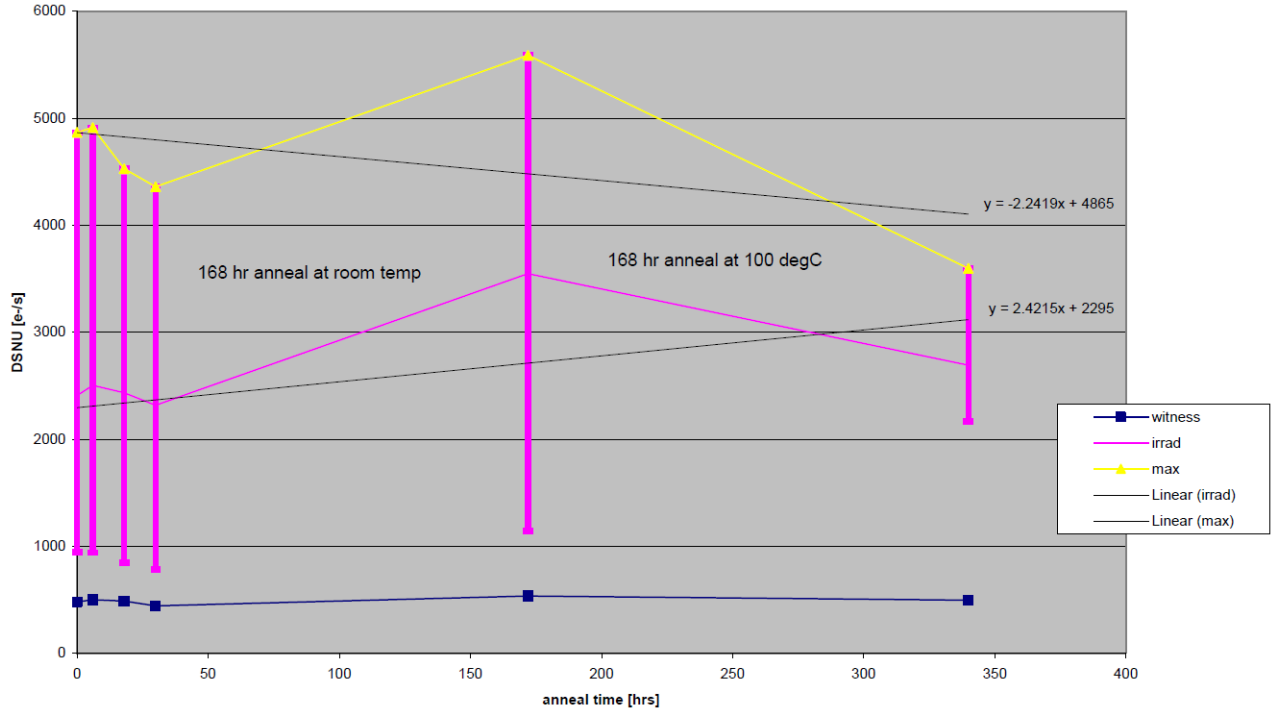


Figure 15. STAR1000 Dark Signal Non Uniformity (DSNU) during annealing

Average dark current rise during annealing. On the average, the dark current still increases during annealing. This observation is not in line with the conclusions of J. Bogaerts. However, during this test the samples were annealed under bias while in the first test the samples were annealed without bias.

Average dark current rise under annealing	221 e-/s per Krad
Maximum dark current rise under annealing	183 e-/s per Krad

The average DSNU remains constant during annealing. It was observed that the average DSNU slightly rises during annealing at room temperature, immediately after irradiation but decreases at elevated temperature. The net effect is almost constant.

Average DSNU rise during annealing	2 e-/s per Krad
Maximum-DSNU rise during annealing	-2 e-/s per Krad (See Note)

NOTE: The spread in DSNU between samples decreases during annealing at temperature.

APPENDIX D: ACRONYMS

Acronym	Description
ADC	analog-to-digital converter
AFE	analog front end
BL	black pixel data
CDM	Charged Device Model
CDS	correlated double sampling
CMOS	complementary metal oxide semiconductor
CRC	cyclic redundancy check
DAC	digital-to-analog converter
DDR	double data rate
DFT	design for test
DNL	differential nonlinearity
DS	Double Sampling
DSNU	dark signal nonuniformity
EIA	Electronic Industries Alliance
ESD	electrostatic discharge
FE	frame end
FF	fill factor
FOT	frame overhead time
FPGA	Field Programmable Gate Array
FPN	fixed pattern noise
FPS	frames per second
FS	frame start
HBM	Human Body Model
IMG	regular pixel data
INL	integral nonlinearity

Acronym	Description
IP	intellectual property
LE	line end
LS	line start
LSB	least significant bit
LVDS	low-voltage differential signaling
MBS	mixed boundary scan
MSB	most significant bit
PGA	programmable gain amplifier
PLS	parasitic light sensitivity
PRBS	pseudo-random binary sequence
PRNU	pixel random nonuniformity
QE	quantum efficiency
RGB	red green blue
RMA	Return Material Authorization
RMS	root mean square
ROI	region of interest
ROT	row overhead time
S/H	sample and hold
SNR	signal-to-noise ratio
SPI	serial peripheral interface
TBD	to be determined
TIA	Telecommunications Industry Association
T_J	Junction Temperature
TR	training pattern
% RH	Percent Relative Humidity

APPENDIX E: GLOSSARY

conversion gain	A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron (1.602E 19 Coulomb) and C is the capacitance of the photodiode or sense node.
DNL	Differential nonlinearity (for ADCs)
DSNU	Dark signal nonuniformity. This parameter characterizes the degree of nonuniformity in dark leakage currents, which can be a major source of fixed pattern noise.
fill-factor	A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured.
INL	Integral nonlinearity (for ADCs)
IR	Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm.
Lux	Photometric unit of luminance (at 550 nm, 1lux = 1 lumen/m^2 = 1/683 W/m^2)
pixel noise	Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane.
photometric units	Units for light measurement that take into account human physiology.
PLS	Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes.
PRNU	Photo-response nonuniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination.
QE	Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent.
read noise	Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal.
reset	The process by which a pixel photodiode or sense node is cleared of electrons. ”Soft” reset occurs when the reset transistor is operated below the threshold. ”Hard” reset occurs when the reset transistor is operated above threshold.
reset noise	Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS.
responsivity	The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
ROI	Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane.
sense node	In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself.
sensitivity	A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m^2)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux is equal to 1 W/m^2; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
spectral response	The photon wavelength dependence of sensitivity or responsivity.
SNR	Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency.
temporal noise	Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels.

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